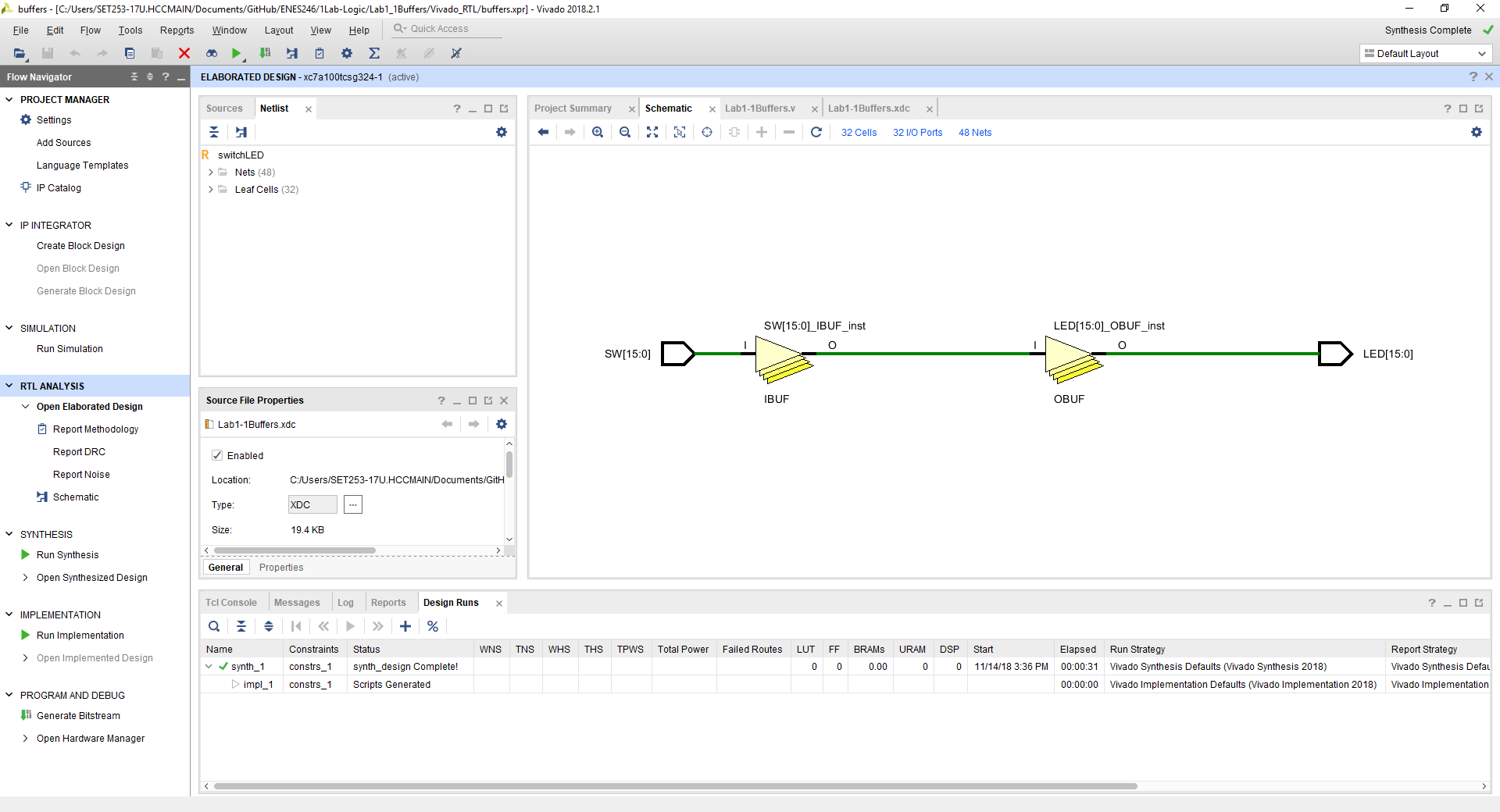
Lab1\_1

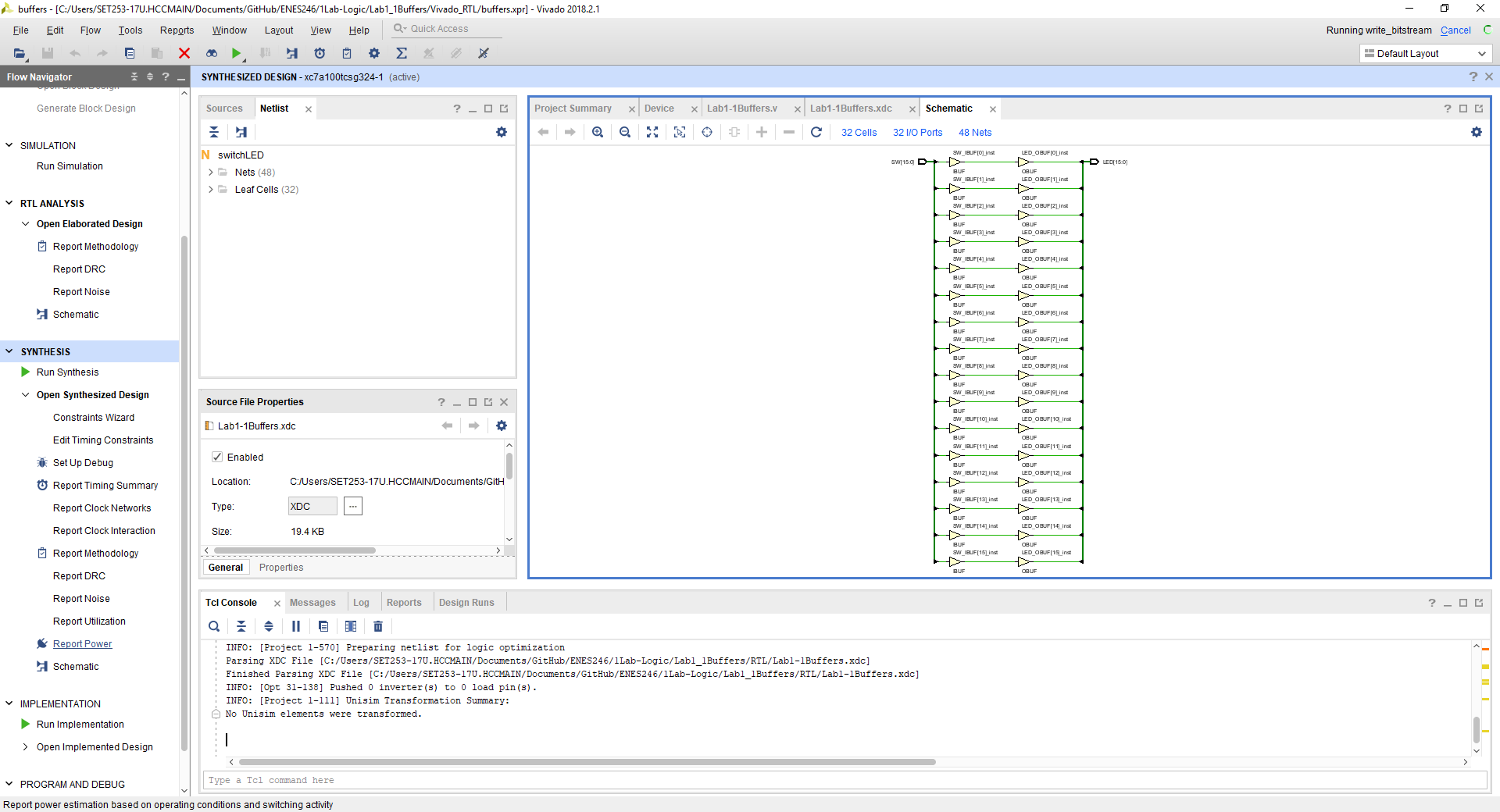
Verilog Code

module switchLED(  
 input [15:0] SW,  
 output [15:0] LED  
 );  
 assign LED = SW;  
endmodule

RTL Analysis Schematic of Lab1\_1Buffers

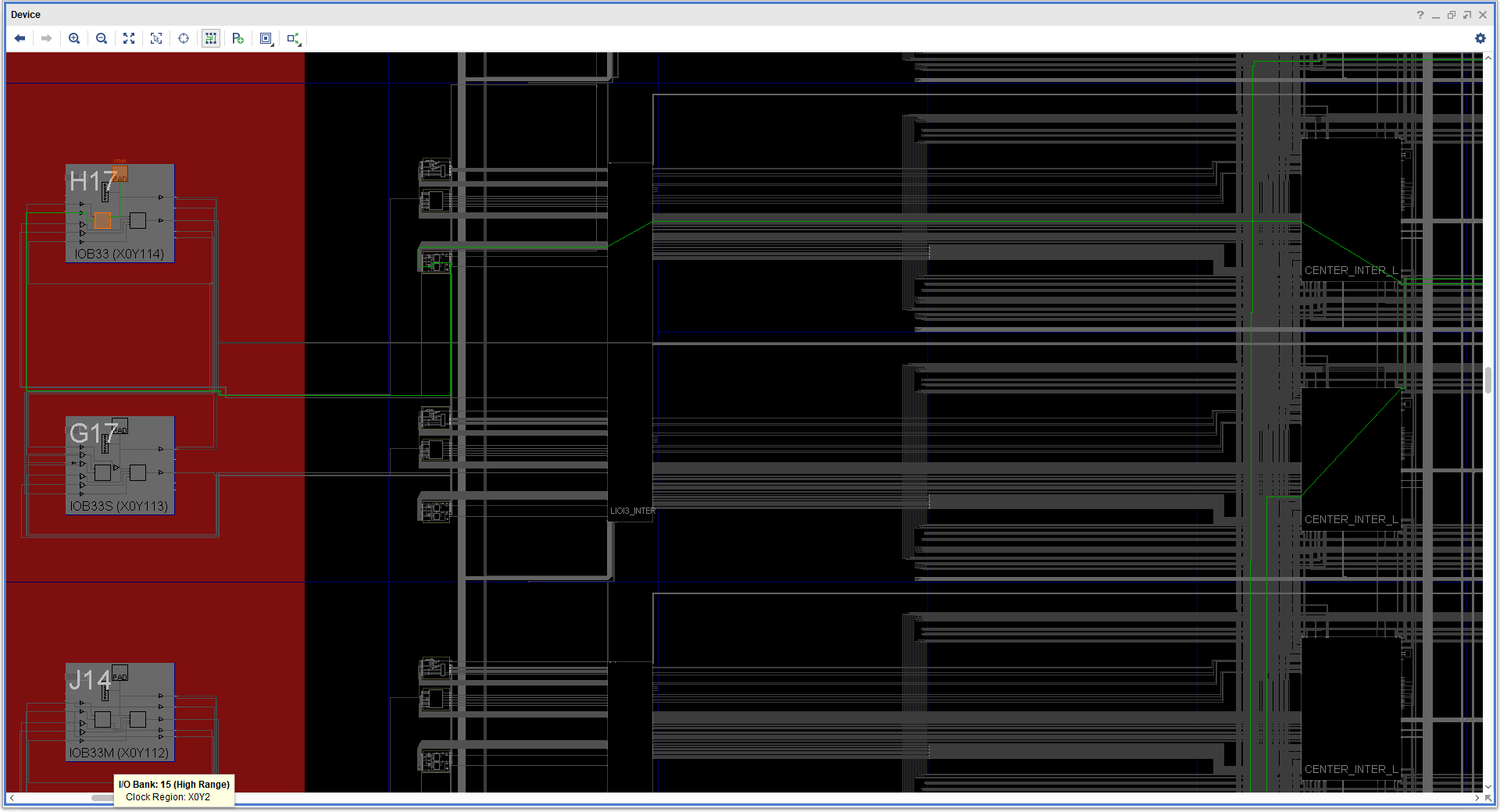


Synthesis Schematic of Lab1\_1Buffers



Comments, the triangle symbols are those of buffers the left pointing box with wire coming out are switches or inputs. The left pointing boxes with wire coming into it are outputs.

Implementation of Lab1\_Buffers



H17 is LED[0] .. can see the green lines that go to the switch that drives it. Can see H17 in the xdc constraints file.

Testing

Manually test by moving each slide switch. The LED above it should turn off or on.